IN THE CLAIMS

1. (Currently Amended) A planar NROM transistor comprising:

an ultra-thin silicon-on-insulator layer having two source/drain regions separated by a normally fully depleted body region;

first and second oxide layers, each formed above a different one of the source/drain regions, the first and second oxide layers laterally separated from each other;

a gate insulator formed over the body region and the first and second oxide layers, the gate insulator capable of storing a plurality of charges in different locations of the insulator; and

a control gate formed on the gate insulator.

2. (Original) The transistor of claim 1 wherein the gate insulator is an oxide-nitride-oxide composite structure.

3. (Original) The transistor of claim 1 wherein the gate insulator layer is a composite layer comprised of one of an oxide-nitride-aluminum oxide composite layer, an oxide-aluminum oxide-oxide composite layer, or an oxide-silicon oxycarbide-oxide composite layer.

4. (Original) The transistor of claim 1 wherein the gate insulator layer is a non-composite layer comprised of one of silicon oxides formed by wet oxidation and not annealed, silicon-rich oxides with inclusions of nanoparticles of silicon, silicon oxynitride layers, silicon-rich aluminum oxide insulators, silicon oxycarbide insulators, or silicon oxide insulators with inclusions of nanoparticles of silicon carbide.

5. (Original) The transistor of claim 1 wherein the gate insulator is comprised of non-stoichiometric single layers of two or more of silicon, nitrogen, aluminum, titanium, tantalum, hafnium, lanthanum, or zirconium.

6. (canceled)

7. (Original) The transistor of claim 1 wherein the transistor has a NAND architecture.

8. (Original) The transistor of claim 1 wherein the transistor has a NOR architecture.

9. (Currently Amended) A planar NROM flash memory cell comprising:

a substrate comprising an insulator layer and a silicon-on-insulator layer that has a thickness less than 100 nm, the silicon-on-insulator layer comprising two source/drain regions separated by a normally fully depleted body region;

first and second oxide layers, each formed above a different one of the source/drain regions, the first and second oxide layers laterally separated from each other;

a composite gate insulator formed over the body region and the first and second oxide layers, the gate insulator having a nitride layer capable of storing a first charge in a first location when the cell is operated in a first direction and a second charge in a second location when the cell is operated in a second direction; and

a control gate formed on the composite gate insulator.

10. (Original) The cell of claim 9 wherein the control gate is comprised of a polysilicon material.

11. (Original) The cell of claim 9 wherein a first source/drain regions operates as a drain region when the cell is operated in the first direction and as a source region when the cell is operated in the second direction.

12 – 22. (Canceled)

23. (Currently Amended) An electronic system comprising:

a processor that generates control signals for the system; and

a memory array coupled to the processor and having a plurality of memory cells comprising:

a planar ultra-thin silicon-on-insulator layer having two source/drain regions separated by a normally fully depleted body region;

first and second oxide layers, each formed above a different one of the source/drain regions, the first and second oxide layers laterally separated from each other;

a gate insulator formed over the body region and the first and second oxide layers, the gate insulator capable of storing a plurality of charges in different locations in the insulator; and

a control gate formed on the gate insulator.

24– 32. (Canceled)

33. (New) The electronic system of claim 23 wherein the gate insulator is an oxide-nitride-oxide composite structure.

34. (New) The electronic system of claim 23 wherein the gate insulator layer is a composite layer comprised of one of an oxide-nitride-aluminum oxide composite layer, an oxide-aluminum oxide-oxide composite layer, or an oxide-silicon oxycarbide-oxide composite layer.

35. (New) The electronic system of claim 23 wherein the gate insulator layer is a non-composite layer comprised of one of silicon oxides formed by wet oxidation and not annealed, silicon-rich oxides with inclusions of nanoparticles of silicon, silicon oxynitride layers, silicon-rich aluminum oxide insulators, silicon oxycarbide insulators, or silicon oxide insulators with inclusions of nanoparticles of silicon carbide.

36. (New) The electronic system of claim 23 wherein the gate insulator is comprised of non-stoichiometric single layers of two or more of silicon, nitrogen, aluminum, titanium, tantalum, hafnium, lanthanum, or zirconium.

37. (New) The electronic system of claim 23 wherein the memory array has a NAND architecture.

38. (New) The electronic system of claim 23 wherein the memory array has a NOR architecture.

39. (New) The electronic system of claim 23 wherein the control gate is comprised of a polysilicon material.

40. (New) The electronic system of claim 23 wherein the first source/drain regions operates as a drain region when the cell is operated in a first direction and as a source region when the cell is operated in a second direction.